FEATURES

- ●Vcc operation voltage: 2.4V ~ 5.5V
- ●Very low power consumption
  - Vcc = 3.0V C-grade: 10.5mA (@55ns) operating current
    I -grade: 11.5mA (@55ns) operating current
    15uA(Typ.) CMOS standby current
  - Vcc = 5.0V C-grade: 12mA (@55ns) operating current
    I -grade: 13mA (@55ns) operating current
    16uA(Typ.) CMOS standby current
- ●High speed access time:
  - -55 55ns (Max.) @ Vcc = 2.4V to 5.5V
- ●Automatic power down when chip is deselected
- ●Three state outputs and TTL compatible
- ●Data retention supply voltage as low as 1.5V
- ●Easy expansion with $\overline{CE1}$, CE2, and $\overline{OE}$ options

DESCRIPTION

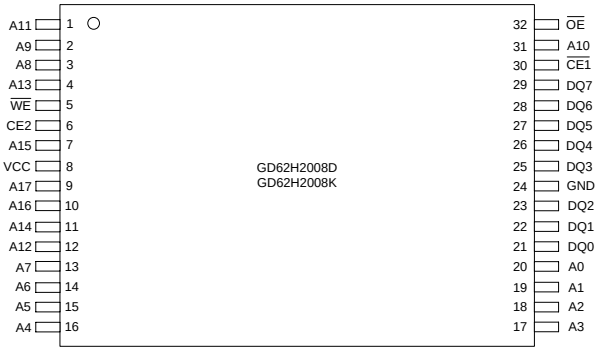
The GD62H2008 is a high performance, very low power CMOS Static Random Access Memory organized as 262,144 by 8 bits and operates from a range of 2.4V to 5.5V supply voltage.

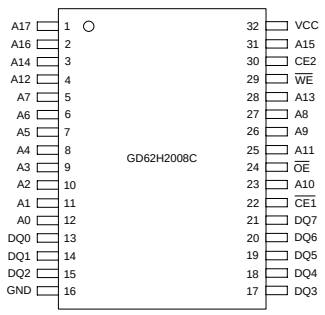
Advanced CMOS technology and circuit techniques provide both high speed and low power features with maximum operation current of 11.5mA at 3.0V and access time of 55ns. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE1}$), an active HIGH chip enable (CE2), and active LOW output enable ($\overline{OE}$) and three-state output drivers. The GD62H2008 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The GD62H2008 is available in JEDEC standard 32 pin Plastic SOP, STSOP and TSOP.

PRODUCT FAMILY

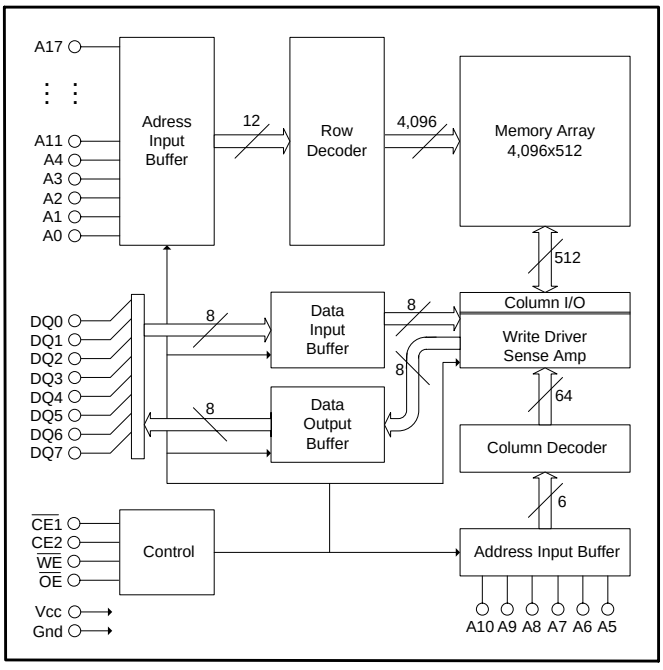
PRODUCT FAMILY	OPERATING TEMPERATURE	OPERATING CURRENT (Max., mA)				STANDBY CURRENT (TYP., uA)		PACKAGE
		55ns		70ns				
		Vcc=3.0V	Vcc=5.0V	Vcc=3.0V	Vcc=5.0V	Vcc=3.0V	Vcc=5.0V	
GD62H2008NC	Commercial 0℃ to +70℃	10.5	12	9	10	15	16	DICE
GD62H2008CC								SOP-32
GD62H2008DC								STSOP-32
GD62H2008KC								TSOP-32
GD62H2008NI	Industrial -40℃ to + 85℃	11.5	13	10	11	15	16	DICE
GD62H2008CI								SOP-32
GD62H2008DI								STSOP-32
GD62H2008KI								TSOP-32

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTIONS

NAME	FUNCTION
A0-A17 Address Input	These 18 address inputs select one of the 262,144 x 8-bit in the RAM
$\overline{CE1}$ Chip Enable 1 Input CE2 Chip Enable 2 Input	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive
DQ0-DQ7 Data Input/Output Ports	These 8 bi-directional ports are used to read data from or write data into the RAM
Vcc	Power Supply
Gnd	Ground

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O OPERATION	Vcc CURRENT
Not selected (Power Down)	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	X	L	X		
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS*

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +85	℃
T_{STG}	Storage Temperature	-60 to +150	℃
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

CAPACITANCE (T_A = 25℃, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (T_A = -40℃ to +85℃)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)			0	--	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)			2.4	--	Vcc	V
I_{IL}	Input Leakage Current	V_{IN} = 0V to Vcc		--	--	1	uA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to Vcc, $\overline{CE1}$= V_{IH}, CE2=V_{IL}, or $\overline{OE}$ = V_{IH}		--	--	1	uA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	Vcc=3.0V	--	--	0.4	V
			Vcc=5.0V				
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	Vcc=3.0V	2.4	--	--	V
			Vcc=5.0V				
I_{CC}	Operating Power Supply Current	$\overline{CE1}$ = V_{IL}, CE2= V_{IH}, I_{DQ} = 0mA, f = $F_{MAX.}$(3)	Vcc=3.0V	--	--	11.5	mA
			Vcc=5.0V	--	--	13	
I_{CCSB}	Standby Current-TTL	$\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, I_{DQ} = 0mA	Vcc=3.0V	--	--	0.5	mA
			Vcc=5.0V	--	--	1.0	
I_{CCSB1}	Standby Current-CMOS	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	Vcc=3.0V	--	15	--	uA
			Vcc=5.0V	--	16	--	

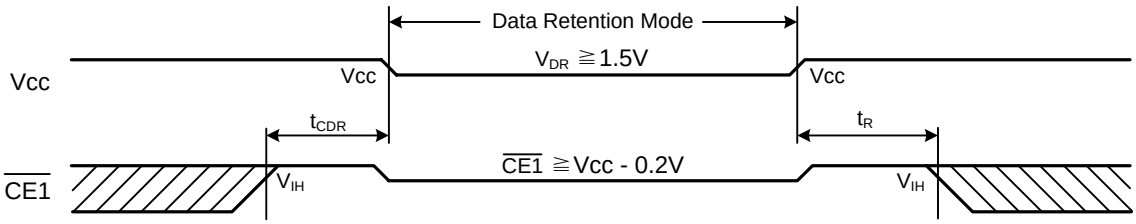
1. Typical characteristics are at T_A = 25℃.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. $F_{MAX.}$ = 1/t_{RC} .

DATA RETENTION CHARACTERISTICS (T_A = -40℃ to +85℃)

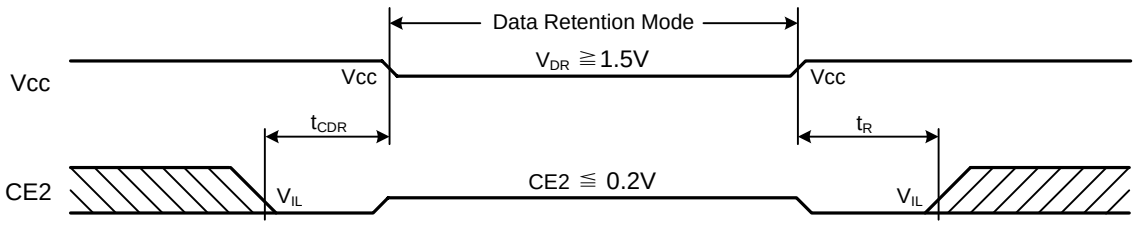
PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.5	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	15	--	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		t_{RC} (2)	--	--	ns

1. Vcc=1.5V, T_A= +25℃
2. t_{RC}= Read Cycle Time

DATA RETENTION WAVEFORM 1 ($\overline{CE1}$ Controlled)

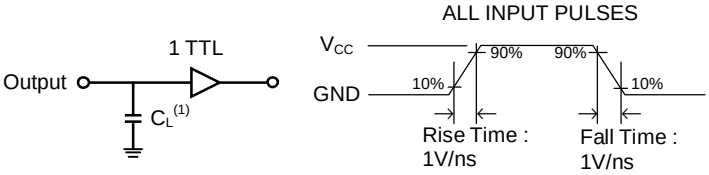


DATA RETENTION WAVEFORM 2 (CE2 Controlled)



AC TEST CONDITIONS

Input Pulse Levels		Vcc/0V
Input Rise and Fall Times		1V/ns
Input and Output Timing Reference Level		0.5Vcc
Output Load	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}	C_L=5pF+1TTL
	Others	C_L=30pF+1TTL



1. Including jig and scope capacitance.

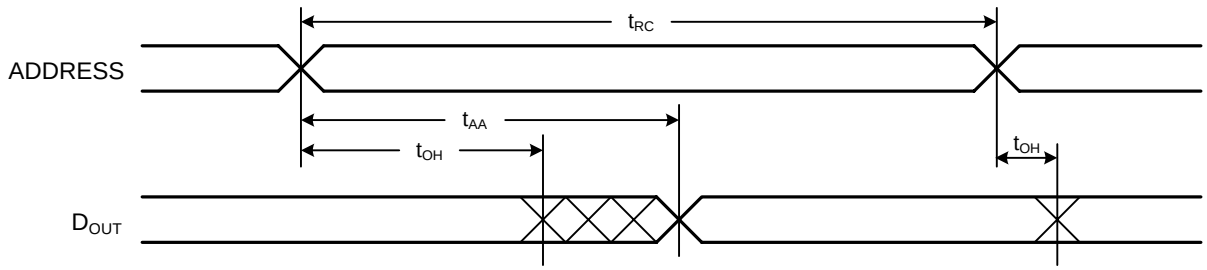
AC ELECTRICAL CHARACTERISTICS (T_A = -40℃ to +85℃, V_{CC}=2.4V~5.5V)

READ CYCLE

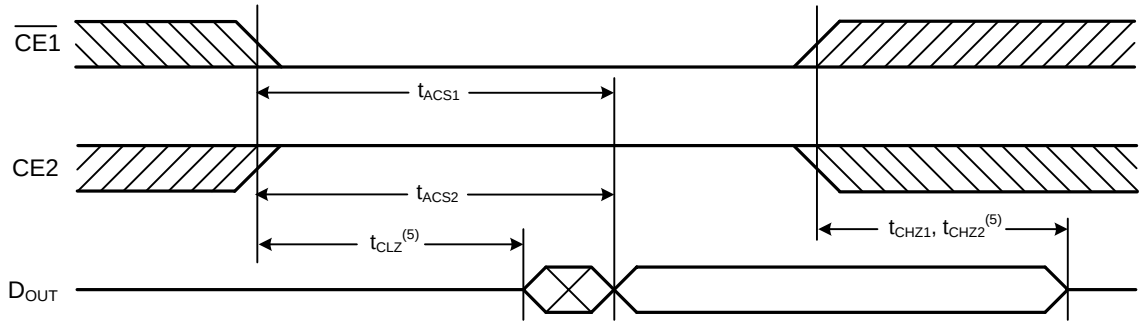
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			CYCLE TIME : 70ns			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	55	--	--	70	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	55	--	--	70	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time ($\overline{CE1}$)	--	--	55	--	--	70	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time (CE2)	--	--	55	--	--	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	30	--	--	35	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z ($\overline{CE1}$)	10	--	--	10	--	--	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to Output Low Z (CE2)	10	--	--	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	5	--	--	5	--	--	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output High Z ($\overline{CE1}$)	--	--	30	--	--	35	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output High Z (CE2)	--	--	30	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output High Z	--	--	25	--	--	30	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	10	--	--	10	--	--	ns

SWITCHING WAVEFORMS (READ CYCLE)

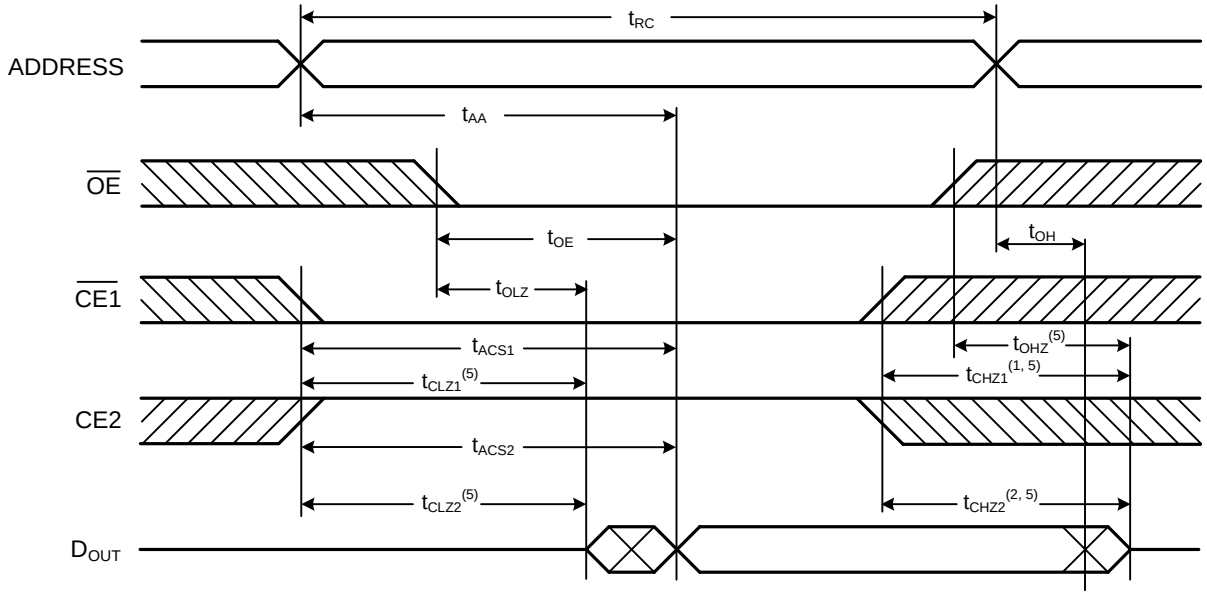
READ CYCLE 1 (1, 2, 4)



READ CYCLE 2 (1, 3, 4)



READ CYCLE 3 (1, 4)



NOTES:

1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE1}$ = V_{IL} and CE2= V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or CE2 transition high.
4. $\overline{OE}$ = V_{IL} .
5. Transition is measured ± 500mV from steady state with C_L=5pF. The parameter is guaranteed but not 100% tested.

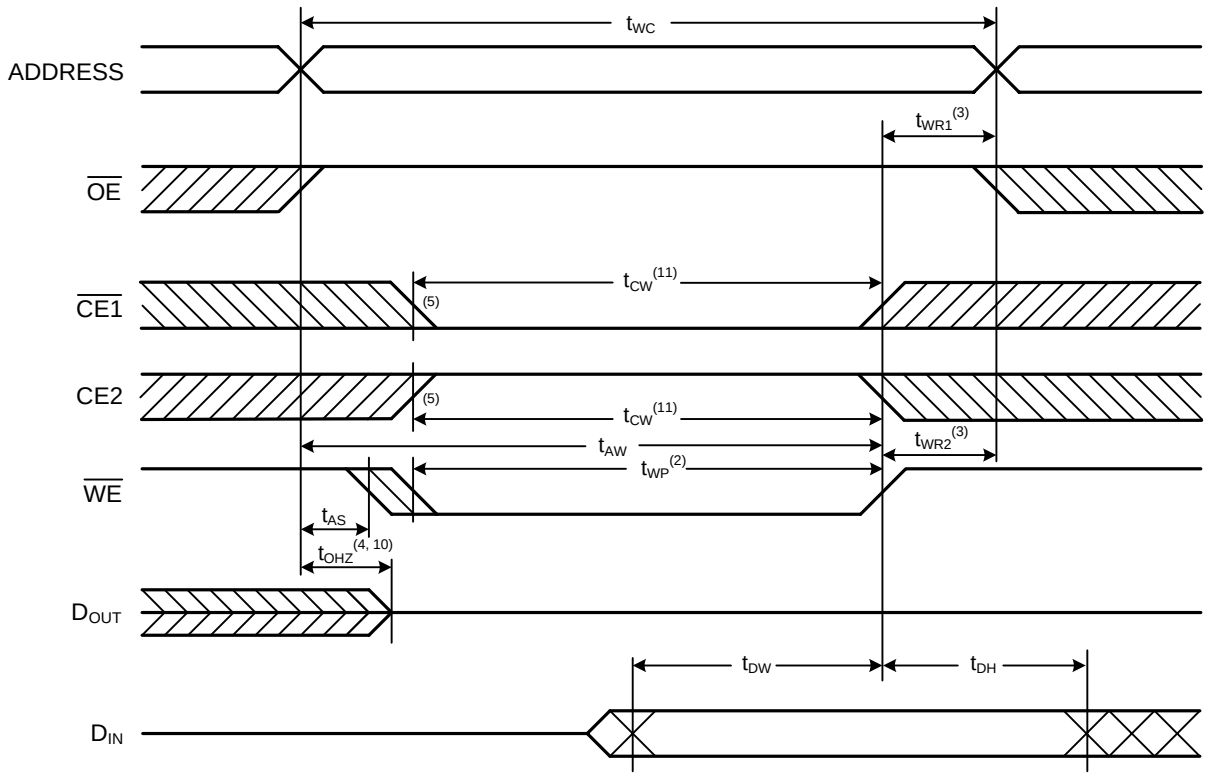
AC ELECTRICAL CHARACTERISTICS (T_A = -40℃ to +85℃, Vcc=2.4V~5.5V)

WRITE CYCLE

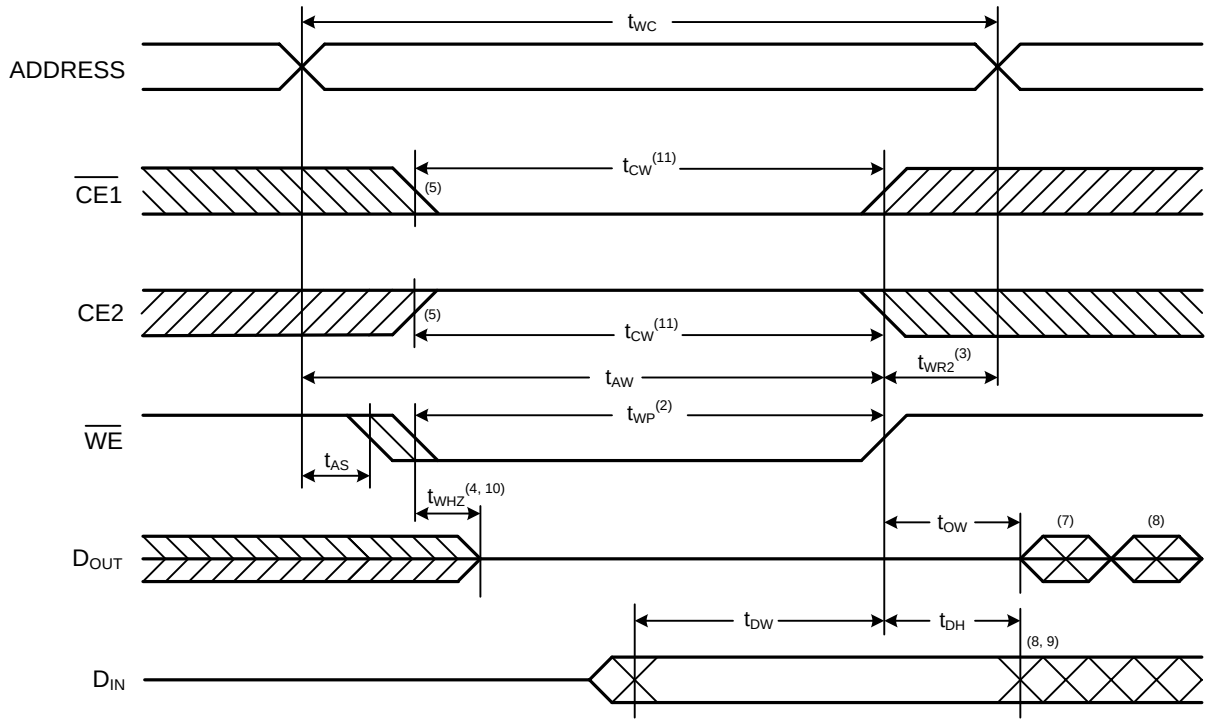
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			CYCLE TIME : 70ns			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	55	--	--	70	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	55	--	--	70	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55	--	--	70	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	30	--	--	35	--	--	ns
t_{WHAX}	t_{WR1}	Write Recovery Time ($\overline{CE1}$, $\overline{WE}$)	0	--	--	0	--	--	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time (CE2)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output High Z	--	--	25	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	--	--	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output High Z	--	--	25	--	--	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	5	--	--	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



WRITE CYCLE 2 (1, 6)

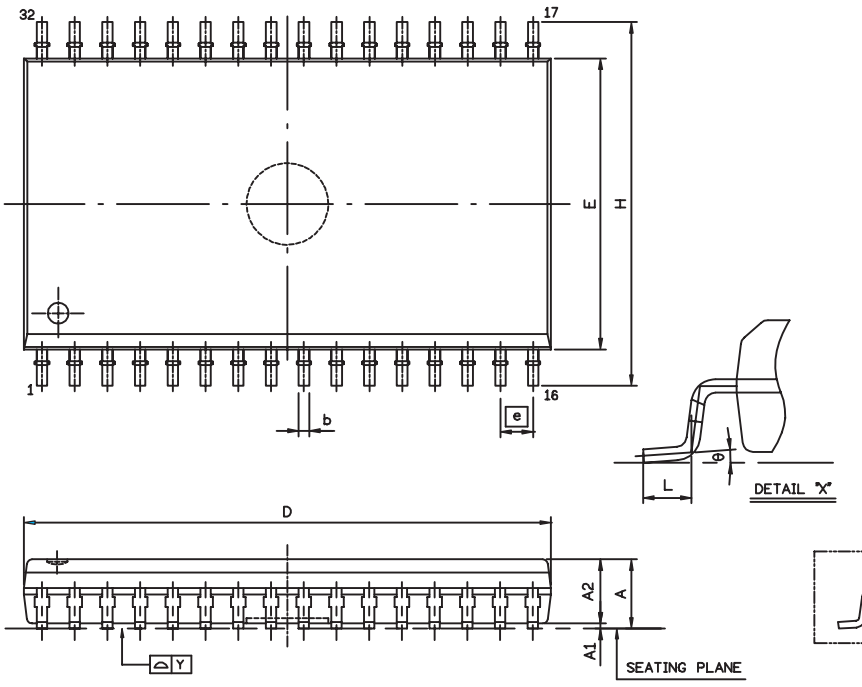


NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remains in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE1}$ is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state with C_L=5pF. The parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

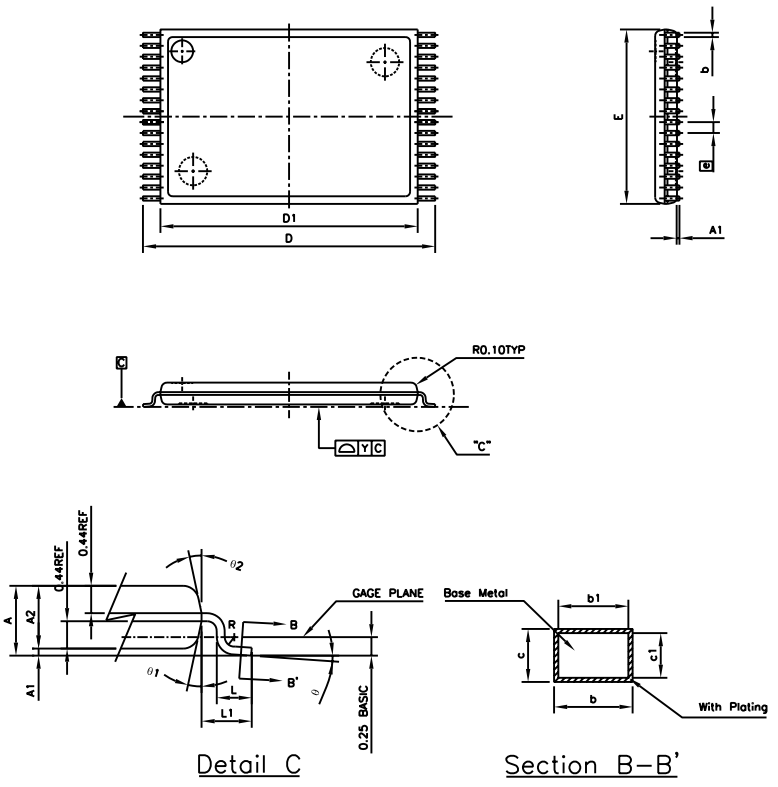
PACKAGE DIMENSIONS

【32-SOP】



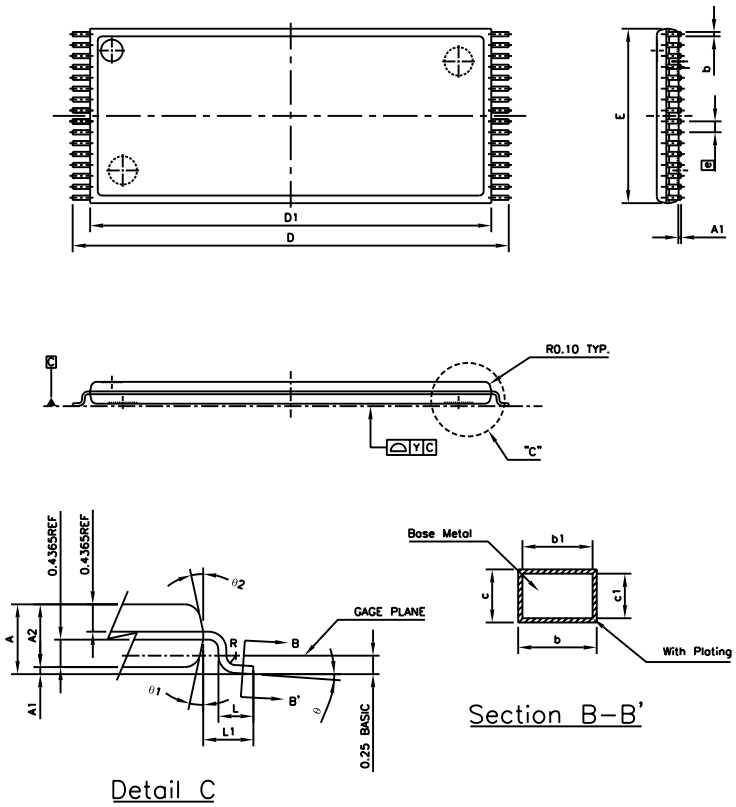
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			2,997			118
A1	0,102			4		
A2	2,565	2,692	2,819	101	106	111
b	0,355	0,406	0,508	14	16	20
c	0,152	0,203	0,305	6	8	12
D		20,447	20,752		805	817
E	11,176	11,303	11,43	440	445	450
e	1,118	1,27	1,422	44	50	56
H	13,868	14,122	14,376	546	556	566
L	0,584	0,787	0,990	23	31	39
L1	1,194	1,397	1,600	47	55	63
Y			0,10			4
θ	0°		10°	0°		10°

【32-STSOP】



SYM.	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.20	–	–	47
A1	0.05	–	0.15	2	–	6
A2	0.95	1.00	1.05	37	39	41
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.10	–	0.21	4	–	8
c1	0.10	–	0.16	4	–	6
D	13.20	13.40	13.60	520	528	535
	0.5 BSC			20 BSC		
D1	11.60	11.80	12.00	457	465	472
E	7.80	8.00	8.20	307	315	323
L	0.50	0.60	0.70	20	24	28
L1	0.80 REF			31 REF		
R	–	–	0.08	–	–	3
θ	0	3°	5°	0	3°	5°
θ1	15° REF			15° REF		
θ2	15° REF			15° REF		

【32-TSOP】



SYM.	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.20	–	–	47
A1	0.05	–	0.15	2	–	6
A2	0.95	1.00	1.05	37	39	41
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.10	–	0.21	4	–	8
c1	0.10	–	0.16	4	–	6
D	19.80	20.00	20.20	780	787	795
e	0.5 BSC			20 BSC		
D1	18.20	18.40	18.60	717	724	732
E	7.80	8.00	8.20	307	315	323
L	0.50	0.60	0.70	20	24	28
L1	0.80 REF			31 REF		
R	–	–	0.08	–	–	3
θ	0	3°	5°	0	3°	5°
θ1	15° REF			15° REF		
θ2	15° REF			15° REF		

Revision History

Rev. No.	History	Date
1.0	Initial draft	Jul. 17, 2007